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Cromemco

4PIO

4 Port I/O Interface

Instruction Manual

Cromemco™

4PIO

INSTRUCTION MANUAL

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Part no. 023-0079

July 1979

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Section 1

INTRODUCTION

The Cromemco 4PIO is an S-100 bus compatible, four isolated I/O port printed circuit board (see Simplified Block Diagram, Figure 1). The 4PIO is designed to operate reliably in high noise industrial control environments where computer system to terminal device electrical isolation is necessary. In summary, the 4PIO features:

* Complete computer system to terminal device electrical isolation.
* Three optically isolated, 8-bit parallel input ports.
* One input port dedicated to 4PIO software status polling.
* Two optically isolated, 8-bit parallel output ports.
* One magnetic relay isolated, 8-bit parallel output port.
* One output port dedicated to software enabling/disabling the other three output ports.
* Optically isolated handshake lines on all three input ports; optically isolated output strobes on the two opto output ports.
* A 5 Kbytes/second opto-isolated parallel data transfer rate.
* Slide switch assigned I/O port address assignments.
* Optically isolated system RESET/NMI (jumper selectable).

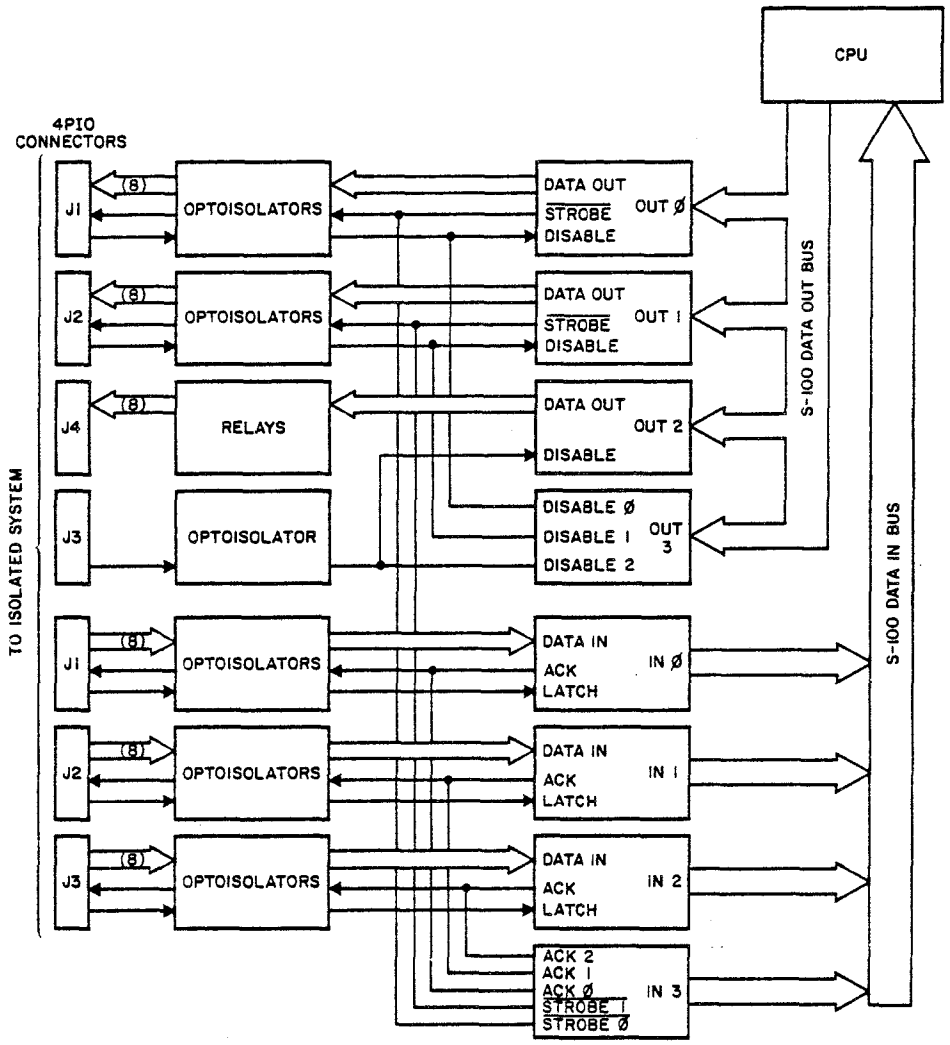


Figure 1: 4PIO BLOCK DIAGRAM

This manual is organized in two basic sections. Section 2, Operating Instructions, supplies all the essential information needed to effectively use and tailor the 4PIO to your specific system requirements. Please read this section carefully and completely to get maximum performance from your 4PIO interface board. Section 3, Assembly Instructions, provides step-by-step assembly and initial board check-out procedures.

4PIO TECHNICAL SPECIFICATIONS

Number of I/O Ports:	4
I/O Port Addresses:	The six high-order port address bits are switch selectable; the two low-order port address bits select one-of-four 4PIO ports
Input Port Functions:	
IN Ø	Inputs opto-isloated 8-bit, parallel data
IN 1	Inputs opto-isolated 8-bit, parallel data
IN 2	Inputs opto-isolated 8-bit, parallel data
IN 3	Polls status of IN Ø, IN 1, IN 2, OUT Ø and OUT 1
Opto-Input Drive:	5 VDC @ 2Ø mA (typ)
Input Handshake Lines:	LATCH INPUT and INPUT ACK
Input Data Set-up Time:	2ØØ uSec (min) before LATCH INPUT
Input Data Hold Time:	1Ø uSec (min) after LATCH INPUT
Output Port Functions:	
OUT Ø	Outputs opto-isolated 8-bit, parallel data
OUT 1	Outputs opto-isolated 8-bit, parallel data
OUT 2	Parallel controls eight SPDT relays
OUT 3	Enable/disable controls OUT Ø, OUT 1, OUT 2
Opto-output Drive:	Ø mA/1.2 mA (min) @ V(ce) = 5 VDC
Output Strobe Timing:	Strobes provided on OUT Ø and OUT 1; PW = 16 uSec; delay = 1Ø4 uSec after data output by CPU
Relay Type:	SPDT
Relay Contact Ratings:	1 Ampere @ 32 VDC or VAC
Bus Compatibility:	S-1ØØ
Power Requirements:	+8 VDC unregulated @ 2.3 A (max)
Operating Environment:	Ø - 55 degrees Celsius

Section 2

OPERATING INSTRUCTIONS

To operate the 4PIO card in your S-100 bus computer system, you must assign the card a Base Address, install interface cabling between the 4PIO and your isolated terminal devices, then write and execute software to control the parallel data transfers between the CPU and the system terminal devices.

2.1 ASSIGNING A 4PIO BASE ADDRESS

The system CPU transfers data between its accumulator (Reg. A) and an I/O port by placing the port address on S-100 bus address lines A0 - A7, and then asserting sOUT true and driving the Data Out lines (DO0 - DO7) if outputting data, or by asserting sINP true and reading the Data In lines (DI0 - DI7) if inputting data. The output sequence is initiated by executing an OUT [port],A instruction, and the input sequence is initiated by executing an IN A,[port] instruction, where "port" is the port address.

The 4PIO is conditioned to respond to four specific port addresses by positioning the six slide switches illustrated in Figure 2. The six switch settings are hardware compared to S-100 bus address lines A7, A6, A5, A4, A3 and A2, thereby defining the 4PIO Base Address. Positioning a Base Address

switch ON causes the 4PIO to respond to a logic 1 level on its corresponding address line; an OFF switch responds to logic Ø (see Figure 3).

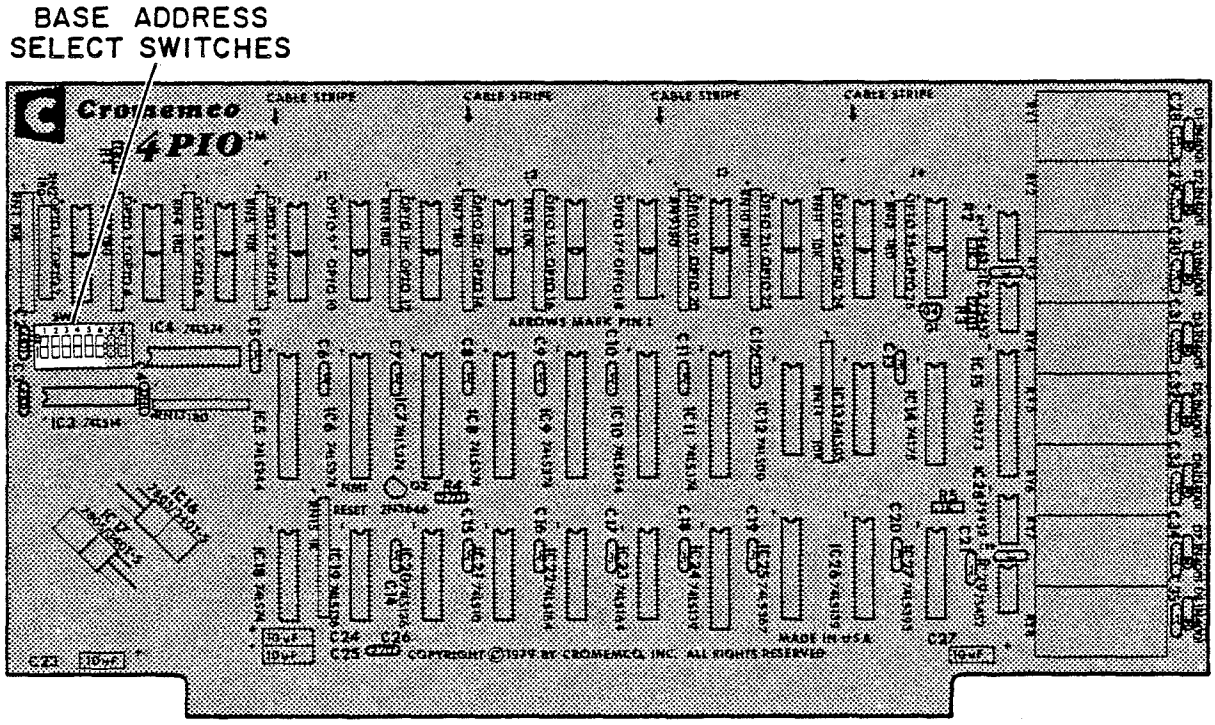


Figure 2: 4PIO BASE ADDRESS SWITCHES

A 4PIO Board Select condition is generated when the CPU asserts either sINP or sOUT, and the Base Address switch settings match the S-1ØØ bus address lines A7 - A2. In this case, the low-order address lines A1 and AØ then select one-of-four 4PIO ports. The two bit number formed by lines A1 and AØ define the port offset from the Base Address. Throughout the remainder of this manual, 4PIO ports will be referenced by their offset. For example, IN Ø and OUT Ø have zero offset from the Base Address, IN 1 and OUT 1 have an

offset of +1 from the Base Address, and so on. An actual 4PIO address is computed by adding the offset to the Base Address.

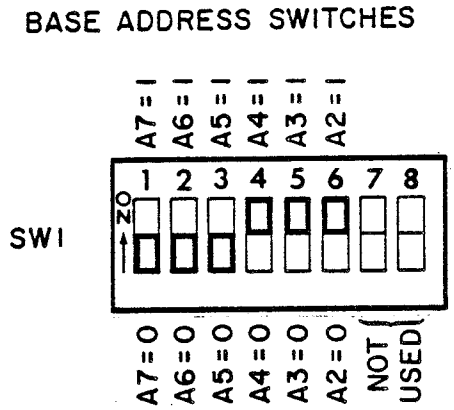


Figure 3: BASE ADDRESS LOGIC LEVELS

EXAMPLE 1

- Setting Base Address switches A7 thru A2 OFF (logic Ø) maps the 4PIO into port addresses ØØH (port Ø) thru Ø3H (port 3).

- Setting Base Address switches A7 thru A2 ON (logic 1) maps the 4PIO into port addresses ØFCH (port Ø) thru ØFFH (port 3).

- Setting Base Address switches A7 thru A5 OFF and A4 thru A2 ON (as in Figure 3) maps the 4PIO into port addresses 1CH (port Ø) thru 1FH (port 3).

If two or more 4PIO cards are installed in the same S-1ØØ bus system, the boards must be assigned distinct and non-overlapping Base Addresses, otherwise a data bus conflict will result when inputting I/O data to the CPU. Also note: Base Addresses ØØH and 3ØH are already used by Cromemco's 4FDC Floppy Disc Controller; 4ØH is used by Cromemco memory boards with BANK SELECT; and 5ØH is used by Cromemco's PRI printer interface. Do not assign the 4PIO a conflicting Base

Address if your system contains any of these Cromemco parts.

After a Base Address has been assigned, the 4PIO may be installed in any empty S-100 bus slot. Always verify that the system power if OFF before inserting or removing the 4PIO from the S-100 bus. Interfacing cables may then be installed connecting 4PIO terminal strips J1 thru J4 to the isolated system terminal devices. After installing interface cabling, parallel data may be transferred between the CPU and your terminal devices under software control.

2.2 4PIO PIN-OUTS & INTERFACE CABLING

Cromemco provides two interface cables which are plug compatible with 4PIO connectors J1 - J4; Part No. 519-0017 (62 cm, $15) and Part No. 519-0018 (110 cm, $15). Each of these cable assemblies consists of a 26-pin female connector which mates with one 4PIO terminal strip connector J1 - J4, a 25-conductor flat ribbon cable of length 62 cm/ 110 cm, and a 25-pin female DB-25S EIA terminating connector. Your I/O terminal devices should be equipped with a mating 25-pin male DB-25P EIA connector when using either of these Cromemco supplied cables.

All J1 - J4 pin numbers referenced in this manual and in the 4PIO schematic correspond to DB-25S EIA pin numbers. Figure 4 illustrates the EIA numbering convention, and also

shows the pin-outs of the 4PIO terminal strips.

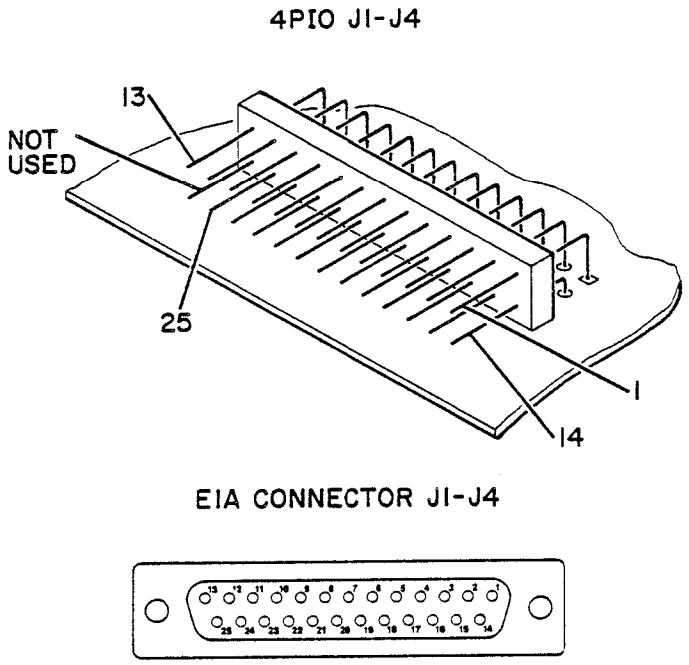


Figure 4: 4PIO PIN NUMBERING

Cromemco supplied cables must be installed by aligning the arrow head near each connector strip on the printed circuit board with the ribbon cable stripe (the colored edge of the ribbon cable. With the cable stripe properly aligned, the pin-outs of EIA connectors J1 thru J4 are shown in Table 1.

Table 1

EIA CONNECTOR J1 THRU J4 PIN-OUTS

Pin	Connector J1	Connector J2	Connector J3	Connector J4
1	-IN Ø BIT DØ	-IN 1 BIT DØ	-IN 2 BIT DØ	OUT 2 BIT DØ (NC)
2	-IN Ø BIT D2	-IN 1 BIT D2	-IN 2 BIT D2	OUT 2 BIT DØ (NO)
3	-IN Ø BIT D4	-IN 1 BIT D4	-IN 2 BIT D4	OUT 2 BIT D1 (POLE)
4	-IN Ø BIT D6	-IN 1 BIT D6	-IN 2 BIT D6	OUT 2 BIT D2 (NC)
5	+IN Ø COMMON	+IN 1 COMMON	+IN 2 COMMON	OUT 2 BIT D2 (NO)
6	+OUT Ø BIT DØ	+OUT 1 BIT DØ	NOT USED	OUT 2 BIT D3 (POLE)
7	+OUT Ø BIT D2	+OUT 1 BIT D2	NOT USED	OUT 2 BIT D4 (NC)
8	+OUT Ø BIT D4	+OUT 1 BIT D4	NOT USED	OUT 2 BIT D4 (NO)
9	+OUT Ø BIT D6	+OUT 1 BIT D6	+RESET/NMI	OUT 2 BIT D5 (POLE)
10	+OUT Ø DISABLE	+OUT 1 DISABLE	+OUT 2 DISABLE	OUT 2 BIT D6 (NC)
11	+LATCH IN Ø	+LATCH IN 1	+LATCH IN 2	OUT 2 BIT D6 (NO)
12	+IN Ø ACK	+IN 1 ACK	+IN 2 ACK	OUT 2 BIT D7 (POLE)
13	+OUT Ø STROBE	+OUT 1 STROBE	NOT USED	NOT USED
14	-IN Ø BIT D1	-IN 1 BIT D1	-IN 2 BIT D1	OUT 2 BIT DØ (POLE)
15	-IN Ø BIT D3	-IN 1 BIT D3	-IN 2 BIT D3	OUT 2 BIT D1 (NC)
16	-IN Ø BIT D5	-IN 1 BIT D5	-IN 2 BIT D5	OUT 2 BIT D1 (NO)
17	-IN Ø BIT D7	-IN 1 BIT D7	-IN 2 BIT D7	OUT 2 BIT D2 (POLE)
18	-OUT Ø COMMON	-OUT 1 COMMON	NOT USED	OUT 2 BIT D3 (NC)
19	+OUT Ø BIT D1	+OUT 1 BIT D1	NOT USED	OUT 2 BIT D3 (NO)
20	+OUT Ø BIT D3	+OUT 1 BIT D3	NOT USED	OUT 2 BIT D4 (POLE)
21	+OUT Ø BIT D5	+OUT 1 BIT D5	NOT USED	OUT 2 BIT D5 (NC)
22	+OUT Ø BIT D7	+OUT 1 BIT D7	-RESET/NMI	OUT 2 BIT D5 (NO)
23	-OUT Ø DISABLE	-OUT 1 DISABLE	-OUT 2 DISABLE	OUT 2 BIT D6 (POLE)
24	-LATCH IN Ø	-LATCH IN 1	-LATCH IN 2	OUT 2 BIT D7 (NC)
25	-IN Ø ACK/ -OUT Ø STROBE	-IN 1 ACK/ -OUT 1 STROBE	-IN 2 ACK	OUT 2 BIT D7 (NO)

These signal lines are functionally grouped and briefly described below. More complete functional descriptions may be found in the manual sections enclosed by parentheses.

INPUT DATA LINES (Section 2.3 & 2.7)

+IN X COMMON:	Common positive terminal, IN port X.
-IN X BIT DZ:	Negative terminal, IN port X, data bit Z. Source current 20 mA = logic 0; source current 0 mA = logic 1.

INPUT HANDSHAKE (Section 2.7 & 2.8)

+/-LATCH IN X:	0 mA to 20 mA transition latches IN port X data.
+/-IN X ACK:	Sink current 1.2 mA [min] when data latched in IN X; sink current 0 mA after CPU reads data from IN X.

OUTPUT DATA LINES (Section 2.3, 2.4 & 2.5)

+OUT X BIT DZ:	Positive terminal, OUT port X, data bit Z. Sink current 1.2 mA (min) = logic 0; sink current 0 mA = logic 1.
OUT 2 BIT DZ (POLE):	Relay data bit Z, relay pole. Output logic 1 to latch relay in energized state; output logic 0 to latch relay in "normal" unenergized state.
OUT 2 BIT DZ (NO):	Relay data bit Z, normally open.
(NO) NORMALLY OPEN:	This contact is not connected to the pole while the relay is off (de energized).
OUT 2 BIT DZ (NC):	Relay data bit Z, normally closed.
(NC) NORMALLY CLOSED:	This contact is connected to the pole while the relay is off (de energized).

OUTPUT CONTROL/HANDSHAKE (Section 2.6 & 2.8)

+/-OUT X DISABLE:	Source current 20 mA unconditionally disables OUT port X; source current 0 mA returns OUT port X to software enable/disable control.
+/-OUT X STROBE:	16 uSec active (sink current = 1.2 mA [min]) pulse, delayed 104 uSec

after data is output to OUT port X by CPU.

CPU CONTROL (Section 2.9)

+/-RESET/NMI: Source current 20 mA generates an S-100 bus pRESET (factory shipped condition) or NMI (jumper wire inserted).

2.3 OPTO-ISOLATOR INTERFACING

Excepting the relays, all data and control is exchanged between the 4PIO and the isolated terminal devices over MCT-66 opto-isolators. This section discusses MCT-66 electrical characteristics and interfacing techniques.

The MCT-66 is a dual optically coupled phototransistor isolator. Each phototransistor consists of an input LED and an optically coupled detector output transistor (see Figure 5 and the MST-66 data sheet, pages 40 and 41). Driving current thru the input LED causes photons to bombard the base region of the output transistor, bringing it into its conduction region. When no current flows thru the input LED, the output transistor receives no base drive, and thus it conducts no collector current.

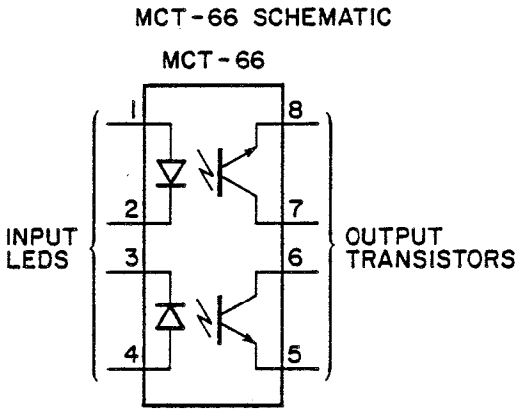


Figure 5: MCT-66 SCHEMATIC

The 4PIO drives the input LEDs when an MCT-66 is used as an output device. In such cases, the LED drive current is either Ø mA (LED OFF) or 2Ø mA (LED ON). When an MCT-66 is used as an input channel, the isolated system must drive the input LED with Ø mA and 2Ø mA (min) - 6Ø mA (max) levels (Cromemco recommends a 2Ø mA ON current for device longevity and maximum switching speed). All 4PIO opto-isolated input channels incorporate a 18Ø ohm series current limiting resistor which anticipates Ø volt and +5 volt drive levels. A typical IN port interface is shown in Figure 6.

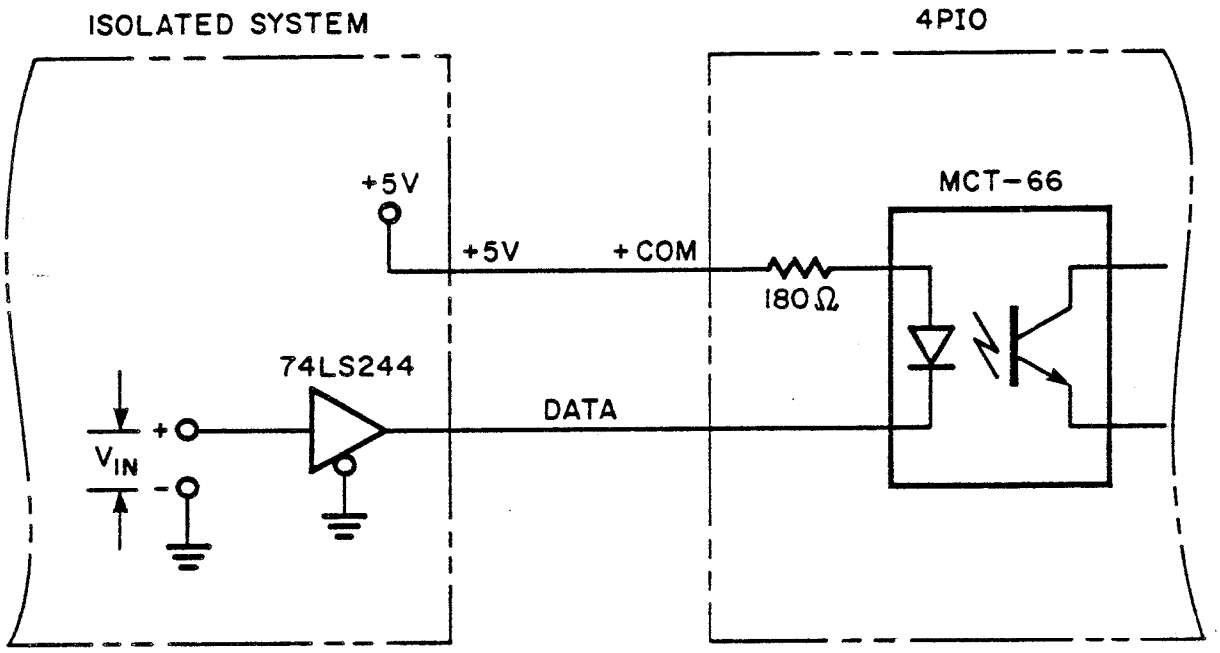


Figure 6: A TYPICAL INPUT MCT-66 INTERFACE

Non-inverting 74LS244 drivers, capable of sinking 24 mA @ +.5 volts, are used in the example interface. Inputting logic Ø to the 74LS244 results in 2Ø mA of LED current, an ON output phototransistor, and thus logic Ø data to the CPU. A logic 1 data bit results in no LED current, an OFF output phototransistor, and thus logic 1 data to the CPU.

Since there are a total of 31 opto-input channels, the isolated system power supply must be capable of sourcing 31 x 2Ø mA = 62Ø mA of forward LED current when fully loaded.

As stated above, the 4PIO supplies either Ø mA or 2Ø mA of LED drive current when outputting opto status and data. The MCT-66 specifications guarantee a 6%(min) input-to-output current transfer ratio which results in Ø mA and 1.2 mA (min) output collector currents. Representative output transistor characteristic curves are shown in Figure 7 for the Ø mA and 2Ø mA LED current conditions.

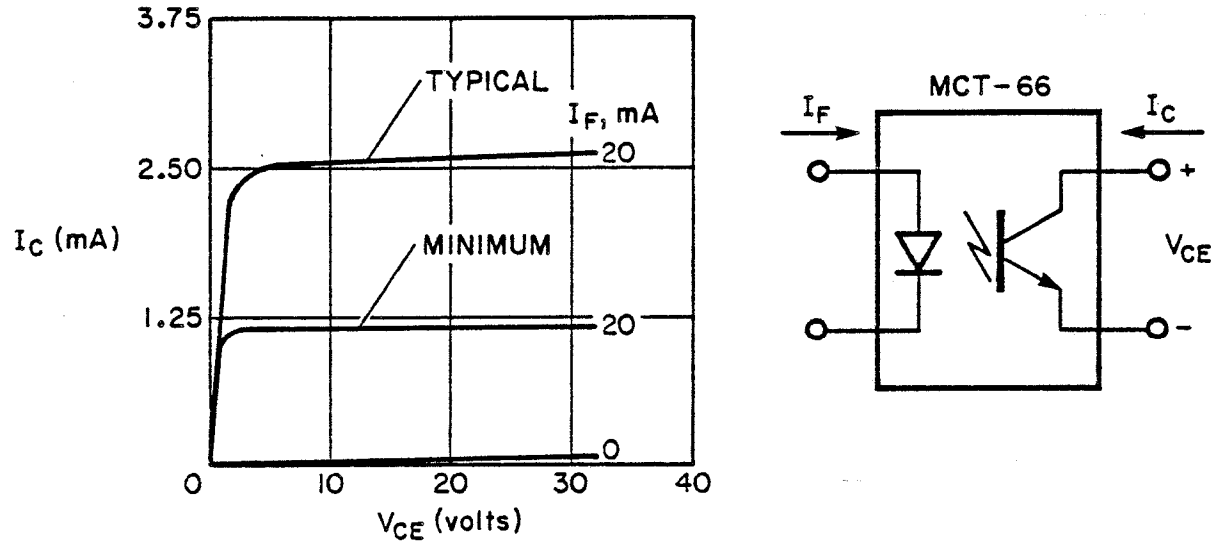


Figure 7: OPTO OUTPUT CHARACTERISTIC CURVES

These characteristic curves suggest a representative OUT port interface illustrated in Figure 8. Notice the MCT-66 output transistors drive low power Schottkey parts with I(IN-LOW) = -Ø.4 mA (max). Since the MCT-66 outputs can sink only 1.2 mA (min), interfacing to standard TTL (-1.6 mA) or Schottkey (-2 mA) is not recommended. The 74LS244 driver inputs are pulled up thru 1ØK resistors to +5 volts to speed up the output transistor turn off time. The pull up resistor value should be small to speed up the RC rise time, but large

enough to limit the MCT-66 sink current to 1.2 mA or less. In general, the pull up resistor value must satisfy:

$$R > [\ V(max) - V(IL)\ ]/[\ 1.2\ mA - I(IL)\ ]$$

where V(max) is the maximum pull up voltage, V(IL) is the maximum input low voltage (+Ø.8 volts for typical 'LS parts), and I(IL) is the maximum input low current (Ø.4 mA for typical 'LS parts).

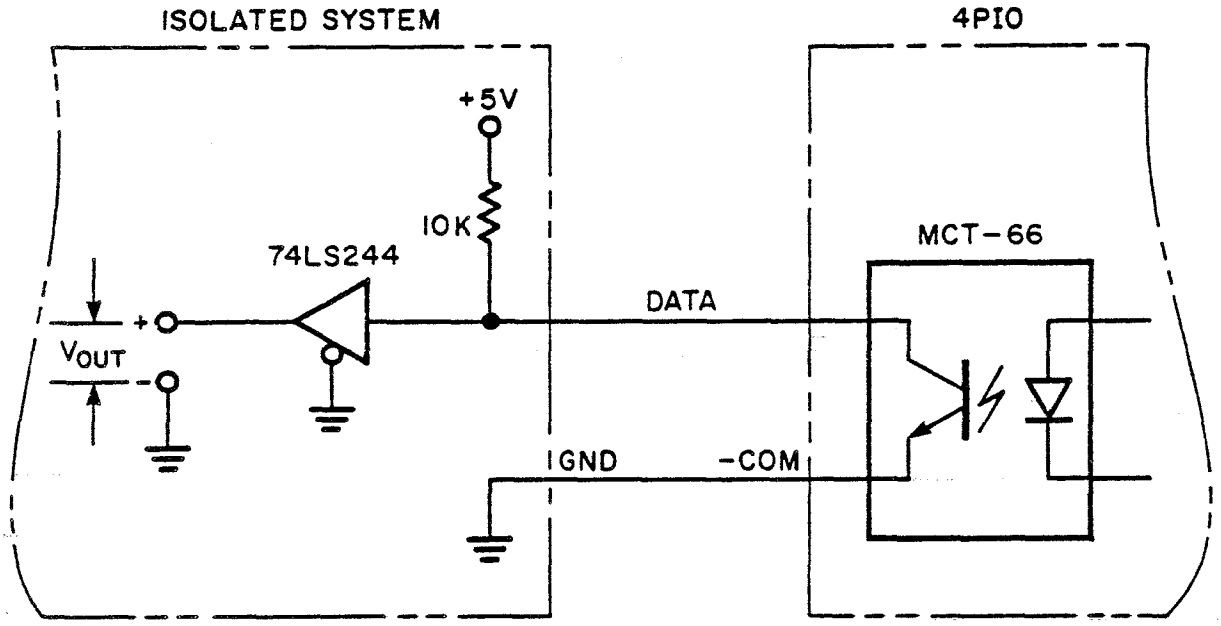


Figure 8: A TYPICAL OUTPUT MCT-66 INTERFACE

The MCT-66 switching times are heavily dependent on the detector output transistor loading. A representative MCT-66 interface and corresponding switching curves are shown in Figure 9.

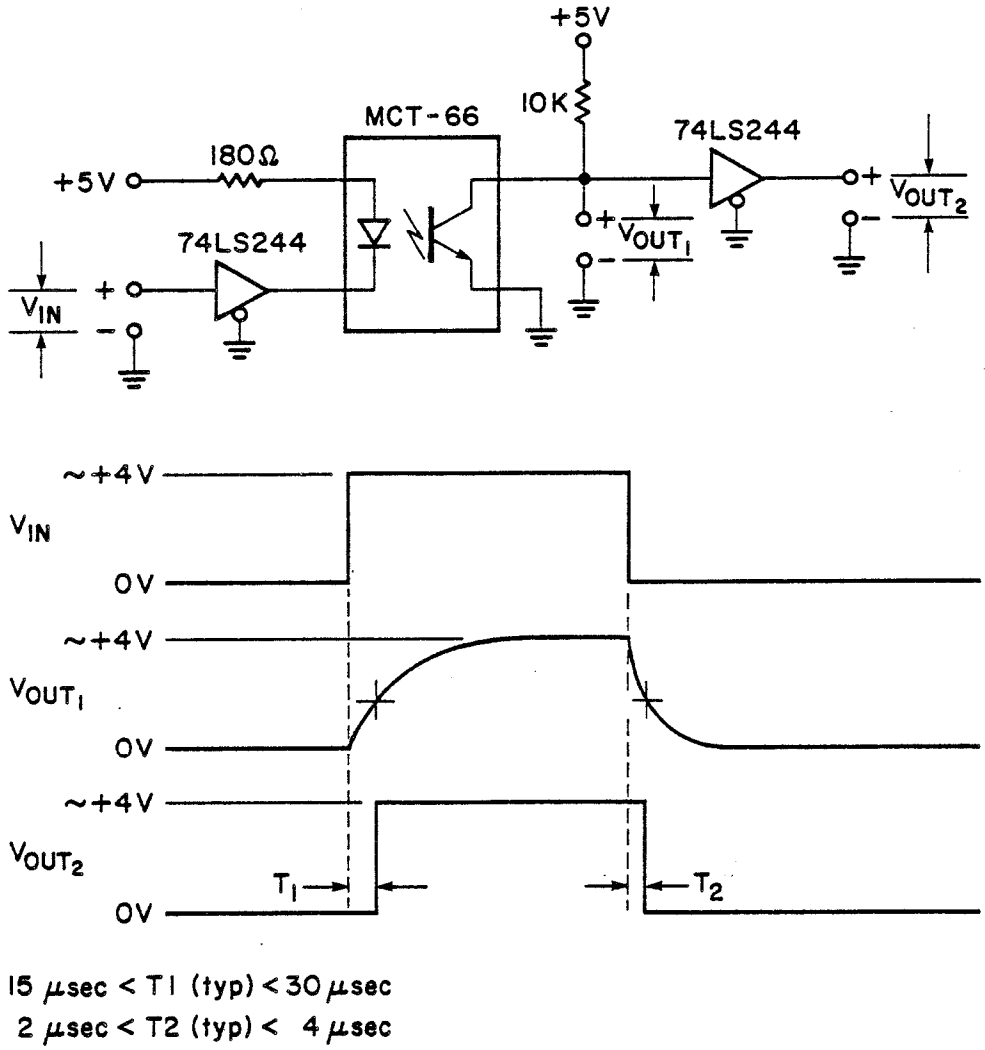


Figure 9: MCT-66 SWITCHING WAVEFORMS

The exponentially rising output transistor turn-off voltage gives rise to T1, the turn-off delay, and the exponentially falling waveform results in T2, the turn-on delay. T1 typically lies between 15 uSec and 30 uSec, while T2 typically lies between 2 uSec and 4 uSec, although infrequently variations of two to three times these typical ranges may be observed.

2.4 OUTPUTTING OPTO-ISOLATED DATA

4PIO ports OUT Ø and OUT 1 output optically isolated, 8-bit parallel data to connectors J1 and J2 respectively. The typical sequence of events when outputting data to either of these ports follows:

(A) The data byte is loaded into CPU register A under program control. A logic 1 data bit results in a high OUT Ø/OUT 1 output voltage (an OFF output transistor); a logic Ø data bit results in a low OUT Ø/OUT 1 output voltage (an ON output transistor).

(B) An OUT [BASE],A instruction is then executed to output the data byte to 4PIO OUT Ø; or an OUT [BASE+1],A is executed to output the data byte to 4PIO OUT 1.

(C) Executing the OUT instruction causes the data byte to be loaded into a 4PIO 8-bit latch (IC7 for OUT Ø; IC9 for OUT 1) during the last clock cycle of the OUT instruction.

(D) The OUT instruction also triggers $\overline{\text{OUTPUT STROBE}}$ circuitry which generates a 16 uSec wide, 104 uSec delayed strobe pulse which indicates to the isolated system that an output data byte is available at the OUT Ø/OUT 1 opto-isolator outputs. The $\overline{\text{OUTPUT STROBE}}$ Ø/1

timing is illustrated below in Figure 1Ø.

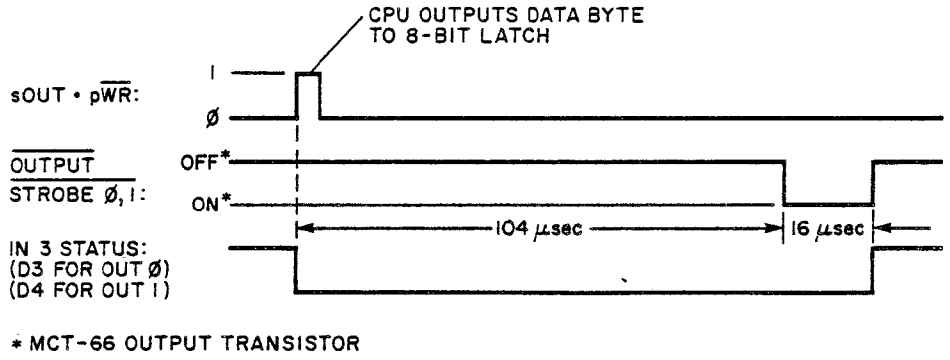


Figure 1Ø: OUT Ø AND OUT 1 STROBE TIMING

(E) The 8-bit latch (IC7 or IC9) drives the opto-isolator inputs as shown in Figure 11. The latch must be brought out of its tri-stated outputs condition by applying an active low level to the $\overline{\text{OUTPUT ENABLE}}$ line, pin 1. This is accomplished by sourcing Ø mA of current to the OUTPUT DISABLE Ø/1 input LED, and by making bit DØ/D1 of 4PIO control port OUT 3 logic 1. See Section 2.6 for a full discussion of control port OUT 3. When the latch outputs are tri-stated, all OUT Ø/OUT 1 MCT-66 output transistors are OFF. When the latch outputs are made active, the data byte bits drive the opto-isolator inputs (logic Ø bits turn MCT-66 output transistors ON; logic 1 bits turn MCT-66 output transistors OFF). The MCT-66 outputs are then coupled to the isolated system as discussed in Section 2.3.

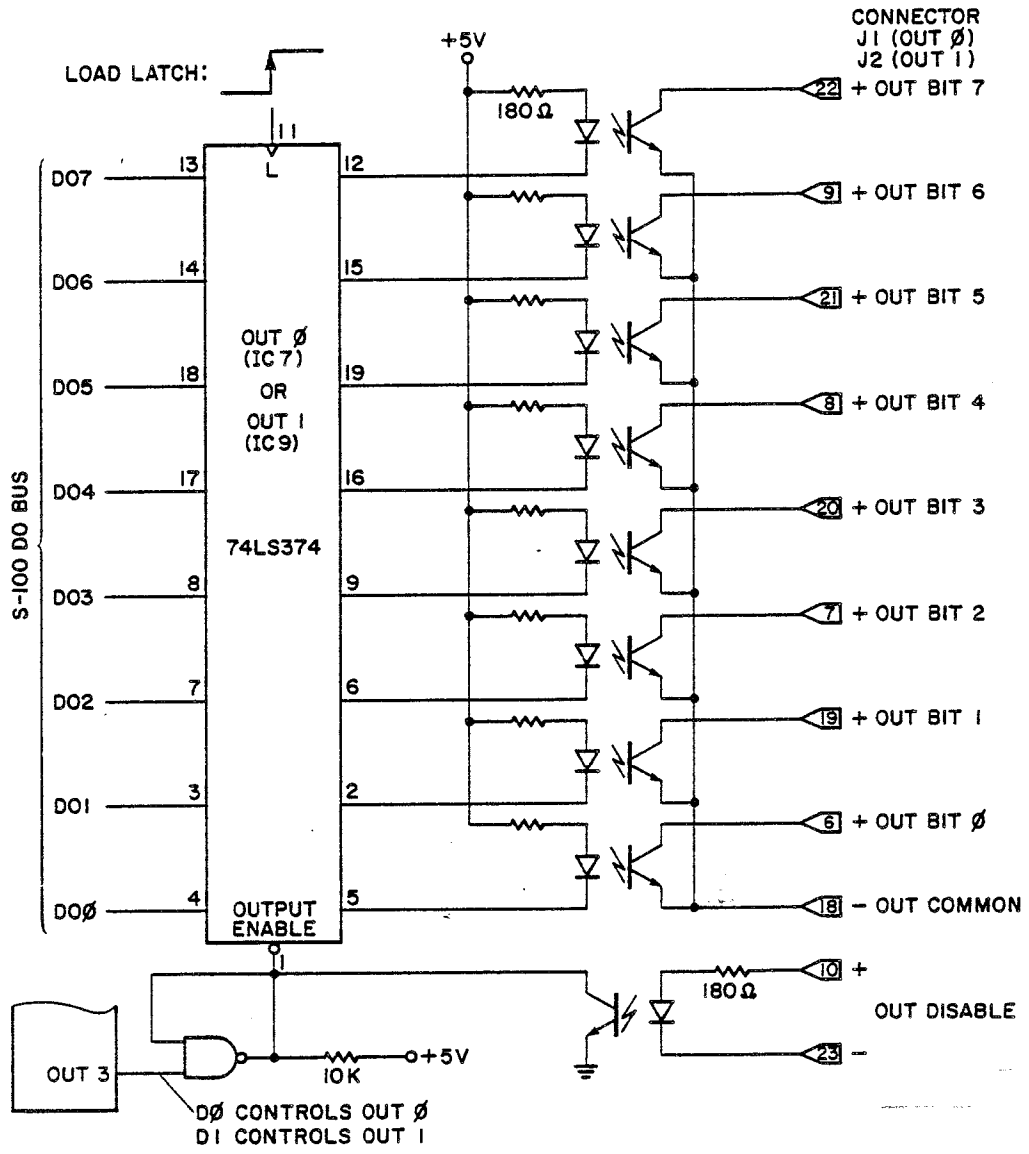


Figure 11: OUT Ø & OUT 1 CIRCUITRY

(F) The isolated system uses handshake line $\overline{\text{OUTPUT STROBE X}}$ (X=Ø,1) as a signal that parallel data is valid at the opto-isolated outputs. Caution: Do not assume output data is valid until $\overline{\text{OUTPUT STROBE X}}$ is active. Either edge of $\overline{\text{OUTPUT STROBE X}}$, or its active low level

may be used to unload the output data to isolated system circuitry.

(G) The CPU monitors bits D3 and D4 of 4PIO status port IN 3 to determine when port OUT Ø or OUT 1 is available to accept new output data (see Figure 1Ø). The 4PIO handshake circuitry anticipates the isolated system will unload the output data during OUTPUT STROBE X, thus the CPU may output new data when OUTPUT STROBE X goes inactive.

2.5 OUT 2 ; RELAY PARALLEL DATA

4PIO port OUT 2 outputs relay isolated, 8-bit parallel data to connector J4. The typical sequence of events to output data to the eight parallel SPDT relays follows: the relay data byte is loaded into CPU register A under program control (a logic 1 data bit energizes its relay, a logic Ø data bit leaves its relay in the "normal" un-energized position); an OUT [BASE+2],A instruction is then executed, where BASE = 4PIO BASE ADDRESS; the OUT instruction loads an 8-bit latch (IC15) with the data byte; the latch contents are then made to actively parallel control four relay drivers (IC1, IC2, IC28 & IC29) only when bit D2 of OUT 3 = logic 1 and OUTPUT DISABLE 2 is inactive (no source current).

Note that the relays may be disabled to their normal, un-energized positions by making bit D2 of OUT 3 = logic Ø

or by making OUTPUT DISABLE 2 active (sourcing 20 mA of current to the input LED). See Section 2.6 for a further discussion of 4PIO control port OUT 3.

EXAMPLE 2

Suppose you have a system with a 4PIO board assigned to Base Address 80H. Further assume the state of your relays is kept as a data byte in memory location RELAYS, and you now want to de-energize RY0, energize RY1 and leave all other relays in their previous state. Executing the program segment below will then accomplish this task:

```
                    ;
                    ; SAMPLE PROGRAM TO DE-ENERGIZE RY0,
                    ; ENERGIZE RY1, AND LEAVE RY2 - RY7
                    ; IN THEIR PREVIOUS STATES.
                    ;
(0080)              BASE:   EQU  80H          ;4PIO BASE ADDRESS
(00FE)              OFMASK: EQU  11111110B    ;TURN OFF RY0
(0002)              ONMASK: EQU  00000010B    ;TURN ON RY1
8000    3A0D80      SAMPLE: LD   A,(RELAYS)   ;GET RELAY DATA
8003    C6FE                AND  A,OFMASK     ;RY0 OFF
8005    F602                OR   A,ONMASK     ;RY1 ON
8007    320D80              LD   (RELAYS),A   ;RESTORE RELAY DATA
800A    D382                OUT  (BASE+2),A   ;DATA TO 4PIO
800C    76                  HALT              ;
800D    00          RELAYS: DB   0            ;ALL OFF INITIALLY
                            END SAMPLE
```

The essential 4PIO logic circuitry effected by this example is shown below in Figure 12. Note that D2 of OUT 3 is assumed at logic 1, and OUTPUT DISABLE 2 source current is assumed 0 mA. Only RY0 and RY1 are shown in their states after program execution.

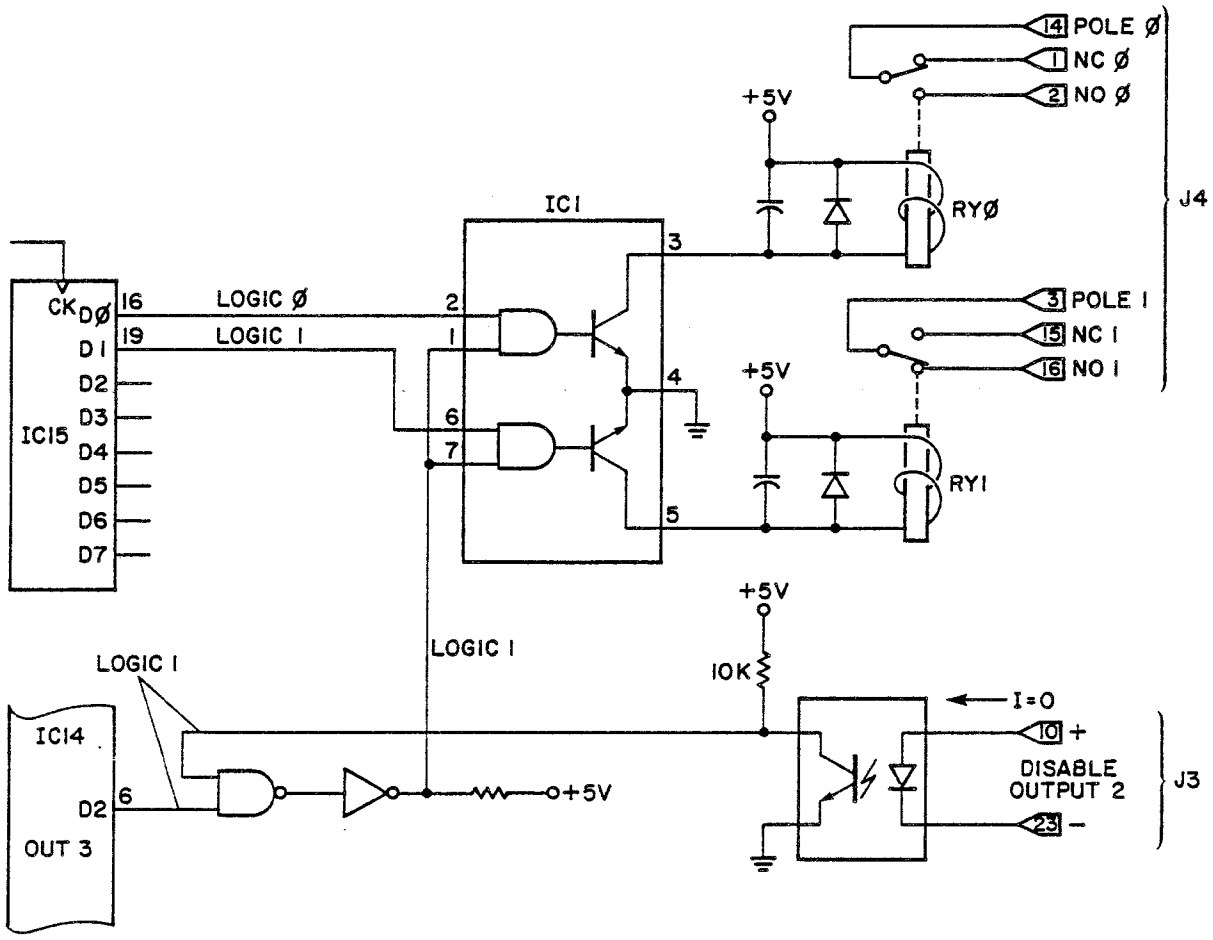


Figure 12: RELAY CONTROL EXAMPLE

2.6 OUT 3 ; OUTPUT PORT ENABLE/DISABLE

4PIO output ports OUT Ø, OUT 1 and OUT 2 are enabled and disabled under a combination of hardware and software control. The 4PIO output states corresponding to the enabled

and disabled conditions are summarized in Table 2 below:

TABLE 2

PORT	CONDITION	4PIO OUTPUT STATE
OUT Ø	ENABLED	LOGIC Ø DATA BIT -> ON MCT-66 TRANSISTOR
		LOGIC 1 DATA BIT -> OFF MCT-66 TRANSISTOR
OUT 1	ENABLED	LOGIC Ø DATA BIT -> ON MCT-66 TRANSISTOR
		LOGIC 1 DATA BIT -> OFF MCT-66 TRANSISTOR
OUT 2	ENABLED	LOGIC Ø DATA BIT -> UN-ENERGIZED RELAY
		LOGIC 1 DATA BIT -> ENERGIZED RELAY
OUT Ø	DISABLED	UNCONDITIONAL OFF MCT-66 TRANSISTORS
OUT 1	DISABLED	UNCONDITIONAL OFF MCT-66 TRANSISTORS
OUT 2	DISABLED	UNCONDITIONAL UN-ENERGIZED RELAYS (NORMAL)

4PIO port OUT 3, bits DØ, D1 and D2, provide software enable/disable control over OUT Ø, OUT 1 and OUT 2 respectively, while opto-isolated input lines OUTPUT DISABLE Ø, OUTPUT DISABLE 1 and OUTPUT DISABLE 2 provide the corresponding hardware control. These control lines are arranged so that a disable from either source disables the corresponding OUT port. Table 3 below summarizes this behavior.

TABLE 3

OUT Port Enable/Disable Control

OUT 3 BIT DX	OUTPUT DISABLE X CURRENT	OUT X STATE
Ø	Ø MA	DISABLED
Ø	2Ø MA	DISABLED
1	Ø MA	ENABLED
1	2Ø MA	DISABLED

WHERE X = Ø, 1 OR 2

Note that only when OUT 3 bit DX is 1 and when OUTPUT DISABLE X current = Ø mA is port OUT X enabled. The corresponding 4PIO enable/disable logic circuitry is shown in Figure 13.

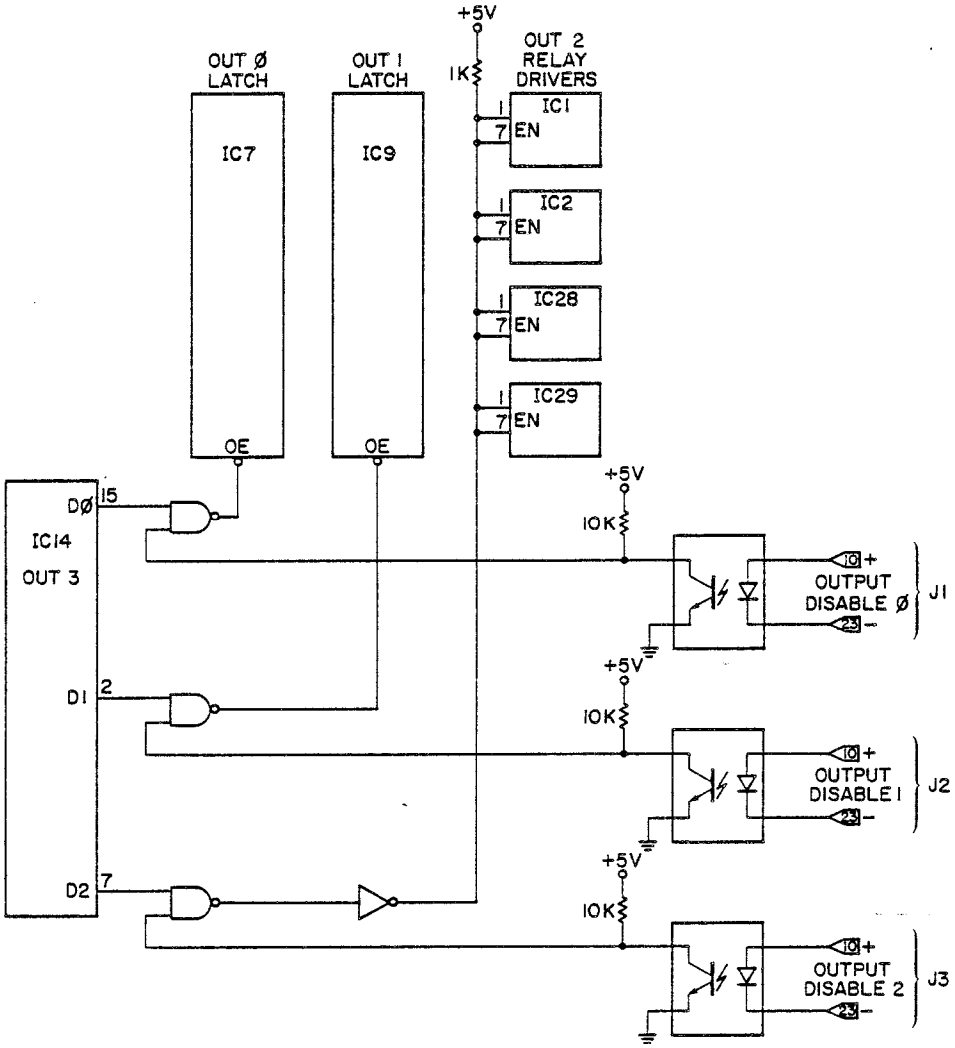


Figure 13: OUT ENABLE/DISABLE LOGIC CIRCUITRY

2.7 IN Ø, IN 1 & IN 2; OPTO PARALLEL IN DATA

4PIO ports IN Ø, IN 1 and IN 2 input optically isolated, 8-bit parallel data from connectors J1, J2 and J3, respectively. The typical sequence of events when inputting parallel data from any of these three ports follows:

(A) The isolated system input device drives eight MCT-66 input LEDs with the parallel data byte (see Section 2.3). An LED drive current of Ø mA inputs a logic 1; a 2Ø mA LED drive current inputs a logic Ø.

(B) After observing a 2ØØ uSec (min) set-up time, the parallel data is loaded into an 8-bit latch (IC6 for IN Ø; IC8 for IN 1; IC11 for IN 2) by sourcing 2Ø mA to control line LATCH INPUT X (X=Ø,1,2) for at least 1Ø uSec. The input data must also observe a 1Ø uSec (min) hold time after LATCH INPUT X goes active (see Figure 14).

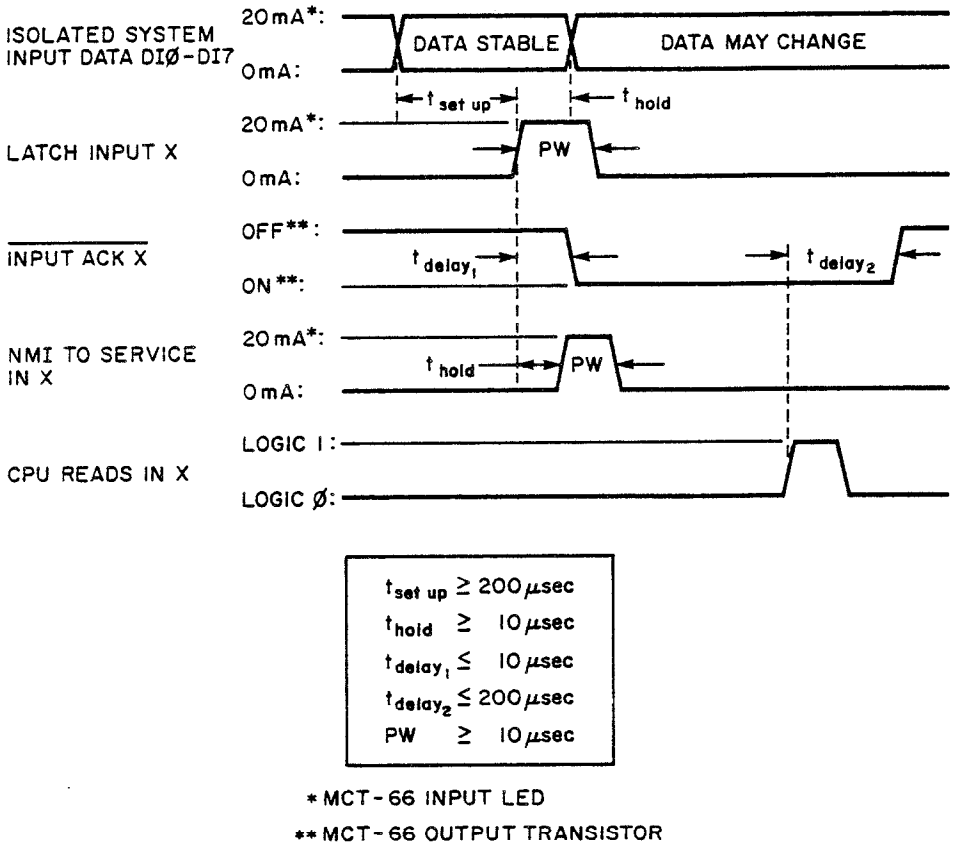


Figure 14: INPUT DATA TIMING REQUIREMENTS

(C) Sourcing 2Ø mA to line LATCH INPUT X activates handshake line $\overline{\text{INPUT ACK X}}$. These three lines are available to the isolated system in inverted form at $\overline{\text{INPUT ACK X}}$ (an ON MCT-66 output transistor acknowledges input data), and to the system CPU in non-inverted form thru port IN 3 (a logic 1 bit acknowledges input data). These lines are reset to their inactive states when the CPU inputs the parallel data from the 8-bit latch. Thus, the isolated system monitors $\overline{\text{INPUT ACK X}}$ to determine when the CPU is ready to accept new input data (see Section 2.8 for full details on staus port IN 3).

(D) The CPU is alerted that input data is available via the Non-Maskable Interrupt (NMI) 4PIO input lines (see Section 2.9), and/or thru polling 4PIO status port IN 3 . The NMI input is optically coupled to S-100 bus line 12, and anticipates a Z80 CPU. When this line goes active low, the Z80 does a restart to a user created service routine starting at memory address 0066H (see Z80 specifications for complete details). Caution: Do not assert NMI active until the input data has satisfied its 10 uSec hold time after LATCH INPUT, otherwise the NMI service routine may read unreliable input data.

(E) The CPU inputs the data byte to register A from port X by executing an IN A,[BASE+X] instruction.

(F) Inputting the data byte clears handshake signal $\overline{\text{INPUT ACK X}}$, thereby alerting the isolated system that new data may be input, and also clearing the corresponding status bit of port IN 3 (see Section 2.8).

2.8 IN 3 ; 4PIO STATUS PORT

4PIO port IN 3 is used to software monitor the ready status of ports IN 0, IN 1, IN 2, OUT 0 and OUT 1 (notice that the relay port, OUT 2, is not monitored by IN 3). The port, implemented in 74LS367 tri-state drivers, connects 4PIO status lines $\overline{\text{INPUT ACK 0}}$, $\overline{\text{INPUT ACK 1}}$, $\overline{\text{INPUT ACK 2}}$, and two shift register output lines from which $\overline{\text{OUT STROBE 0}}$ and $\overline{\text{OUT STROBE 1}}$ are derived, to the S-100 data in (DI) bus as shown

in Figure 15.

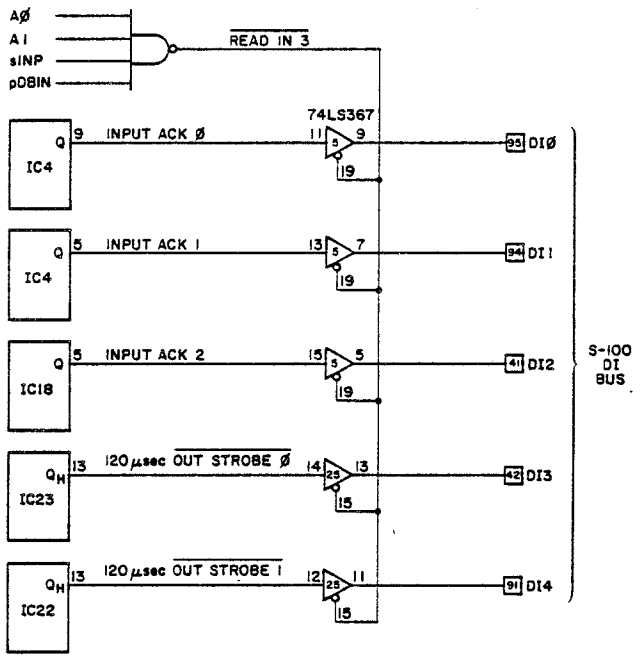


Figure 15: STATUS PORT IN 3

The CPU reads the port contents by executing an IN A,[BASE+3] instruction, and the bits of the read status byte are interpreted as follows:

Table 4

4PIO Status Port IN 3

IN 3 STATUS BIT	4PIO STATUS
DØ = LOGIC Ø	PORT IN Ø EMPTY
DØ = LOGIC 1	PORT IN Ø DATA AVAILABLE
D1 = LOGIC Ø	PORT IN 1 EMPTY
D1 = LOGIC 1	PORT IN 1 DATA AVAILABLE
D2 = LOGIC Ø	PORT IN 2 EMPTY
D2 = LOGIC 1	PORT IN 2 DATA AVAILABLE
D3 = LOGIC Ø	PORT OUT Ø BUSY OUTPUTTING DATA
D3 = LOGIC 1	PORT OUT Ø READY FOR NEW DATA
D4 = LOGIC Ø	PORT OUT 1 BUSY OUTPUTTING DATA
D4 = LOGIC 1	PORT OUT 1 READY FOR NEW DATA
D5, D6, D7	NOT USED

After the system CPU reads port IN Ø, IN 1 or IN 2, its corresponding status bit is reset to indicate empty, although the previous input data remains latched and available for re-reading until over-written by a new input data byte.

2.9 4PIO RESET, POWER-UP & NMI

The 4PIO responds to a system RESET (when S-1ØØ bus line 75 $\overline{\text{pRESET}}$ goes active low) by: clearing any active $\overline{\text{OUT STROBE Ø}}$ or $\overline{\text{OUT STROBE 1}}$; clearing any active $\overline{\text{INPUT ACK Ø}}$, $\overline{\text{INPUT ACK 1}}$, $\overline{\text{INPUT ACK 2}}$; tri-stating both OUT Ø and OUT 1 8-bit latches thereby forcing all OUT Ø and OUT 1 opto-output transistors OFF; and returning all SPDT relays to their normal, un-energized positions. Since many systems automatically generate a RESET upon power-up or after an

intermittent power failure, the post-RESET 4PIO state should then correspond to a "safe", "non-runaway" condition, especially in sensitive control applications.

After system RESET, initialization, or power failure, recovery software would typically configure 4PIO output ports OUT Ø, OUT 1 and OUT 2 by outputting an appropriate control word to OUT 3 (see Section 2.6).

The 4PIO provides an opto-isolated input channel which may be wired to produce either a system RESET, or a Non-Maskable Interrupt (NMI). In its factory wired condition, sourcing 2Ø mA to input lines J3 pins 9 & 22 generates a system pRESET by forcing S-1ØØ bus line 75 active low. Alternately, J3 pins 9 & 22 may be defined as NMI control lines by cutting a trace and installing a jumper wire as illustrated in Figure 16. With the cut trace and the jumper inserted, sourcing 2Ø mA to J3 pins 9 & 22 then generates a NMI by forcing S-1ØØ bus line 12 active low.

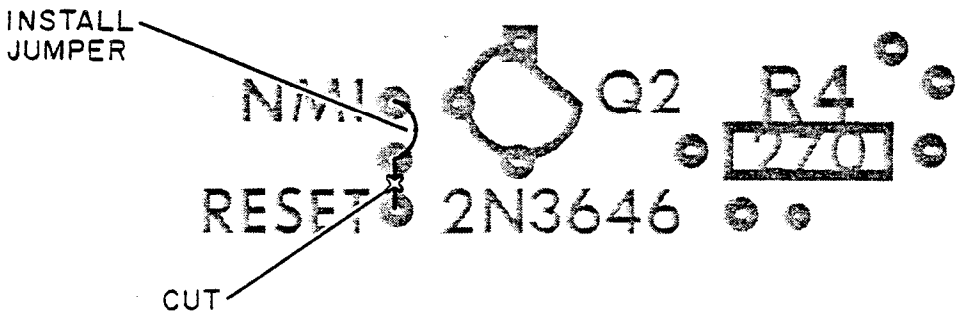


Figure 16: RESET/NMI JUMPER OPTION

Section 3

ASSEMBLY INSTRUCTIONS

If you purchased a 4PIO kit, you will find assembly to be straight forward provided you follow the instructions below. Before beginning assembly, verify you have all kit parts by referring to the 4PIO PARTS LIST near the end of this manual. Please fill out and return the included Missing Parts Form to your authorized Cromemco dealer if any parts are damaged or missing.

3.1 ASSEMBLY STEPS

The following tools will be needed to assemble your 4PIO kit: small needle nosed pliers; small diagonal cutters (dikes); small phillips head screw driver; a fine tipped low-wattage soldering iron (25 W or less); a supply of fine, high quality multi-core rosin solder--DO NOT USE ACID CORE SOLDER; an ohmmeter; flurocarbon cleaning solution; and a de-soldering tool (optional).

All 4PIO parts are inserted from the board component side (with the white printed legend); all soldering is done from the opposite side (the board solder side). For professional looking results, bend component leads at right angles to match the solder pad span before component insertion and soldering. After soldering, trim away excess lead length by cutting as close to the board as possible.

The printed legend on the component side shows the exact location and orientation of each component. You may also find the PARTS LOCATION DIAGRAM helpful when components overlay the printed legend. Follow the steps below in order, checking off each instruction step when completed.

( ) On the board component right side is the relay mounting area. The relays are plugged into female spring sockets which must be soldered to the 40 large feed-thru holes. Using one of the relays as an assembly jig, mount five spring sockets on the relay legs, then push the relay into place until properly seated from the component side. Solder the five sockets in place from the solder side. Unplug the relay and solder the remaining thirty-five sockets in place in a similar fashion.

( ) Solder in position four 1/4 watt resistors:

R1	180	brown-grey-brown
R2	1K	brown-black-red
R3	270	red-violet-brown
R4		Not used
R5	1K	brown-black-red

( ) Install eight diodes D1 - D8. Align diode banded ends with the arrow symbol (anode end) printed legends, and the square pad in the PC foil.

( ) Install four 10 uF polarized tantalum capacitors C23 - C25 and C27. Align the "+" symbol on each capacitor with the "+" legend symbol, and the square pad in the PC foil.

( ) Install three .ØØ1 uF ceramic disc capacitors C2 - C4, and one 22Ø pF capacitor C26.

( ) Install twenty-seven Ø.1 uF capacitors C1, C5 - C22 and C28 - C35.

( ) Install transistor Q1 (2N39Ø4). Note that transistor Q2, labeled a 2N3646 on the board legend, is not used. Align the transistor flat side with outline drawing. The square pad in the PC foil marks the emitter lead.

( ) Install a short piece of insulated jumper wire between the right unused R4 solder pad, and the unused collector solder pad of Q2 (see Figure 17).

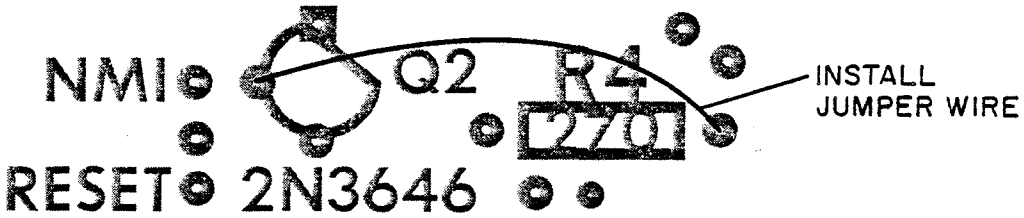


Figure 17: R4 - Q2 JUMPER WIRE PLACEMENT

( ) Install resistor SIP network RN15 (1K, 1Ø pin). The legend arrow symbol points to SIP pin 1 which is marked on the package with either a numeral "1" or a dot, pin 1 is inserted in the square pad in the PC foil.

( ) Likewise, install 8 pin 18Ø ohm SIPs RN2, RN12, RN13; then 1Ø pin 1ØK SIPs RN1, RN5, RN8, RN11, RN14; then 1Ø pin 18Ø ohm SIPs RN3, RN4, RN6, RN7, RN9 and RN1Ø.

( ) Install the eight position DIP switch package SW1. Orient the package so that the ON position in towards the top of the board.

( ) Install four 26-pin cable connector strips J1 - J4. Position each strip so that the right angle bent legs are soldered to the p.c. board, and the straight legs point towards the top of the board.

( ) Mount the large heatsink assembly in the board lower left corner. Insert the phillips head screws from the solder side mating with hex nuts on the component side. Finger tighten.

( ) Install two 78Ø5 +5 volt regulators on the heatsink. Pre-bend the regulator leads to match solder pad spacing, loosely install securing screw (from solder side) and hex nut to each regulator, then solder regulator leads. Make sure the regulator leads do not contact the metallic heat sink assembly. Take care that the triangular holes in the heat sink do not touch any of the pads in the PC foil. Tighten all four screws.

( ) Install four 8-pin IC sockets in positions IC1, IC2, IC28 and IC29.

( ) Install the remaining thirty-six IC sockets.

( ) Connect an ohmmeter, set on the RX1 or lowest range, across C23, then C24, then C25. Verify a near full-scale

reading (several hundered ohms or greater) in each case. If not, a short circuit between +8 volts and ground (C23), or between +5 volts and ground (C24, C25) is indicated. Locate and remove the short circuit, then re-test as above before proceeding.

IMPORTANT NOTE

The most common assembly fault is bent-under IC legs. To avoid this problem, first bend the IC legs to closely match the IC socket span. Then, "rock" the IC into its socket with a gentle end-to-end pressure. Visually inspect the legs after insertion by looking beneath the device.

( ) Install twenty-six MCT-66 opto-isolators in positions OPTO1 - OPTO26. Note that two MCT-66s occupy one 16-pin IC socket. In each case, the legend arrow tip symbol points to IC pin 1 (see Figure 18 below).

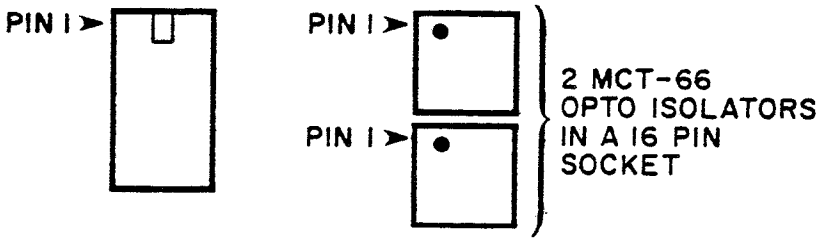


Figure 18:IC PIN 1

( ) Install the remaining thirty-six ICs. Again, the legend arrow tip symbol points to IC pin 1.

( ) Plug eight relays RY1 - RY8 into the female spring sockets soldered in place at the first assembly step.

This completes assembly of your Cromemco 4PIO board. Clean the board solder side with the fluorocarbon solution to remove any fine metallic particles which may be imbedded in the rosin residue. Carefully inspect the solder side for unsoldered pads, or solder bridges between adjacent pads.

If further testing indicates a board failure, the first corrective measure should be the removal of all board ICs to check for bent under IC legs. If none are found, re-insert all ICs paying close attention to correct IC placement, orientation, and insertion. If problems persist, return the board to Cromemco, Inc. for servicing (see WARRANTY at the end of this manual).

4PIO PARTS LIST

Part Description		Part No.
Integrated Circuits		
IC1-2	75452	010-0147
IC3	74LS14	010-0061
IC4	74LS74	010-0055
IC5	74LS244	010-0100
IC6-9	74LS374	010-0133
IC10	74LS244	010-0100
IC11	74LS00	010-0069
IC12	74LS374	010-0133
IC13	74LS05	010-0065
IC14	74175	010-0006
IC15	74LS273	010-0107
IC16-17	7805	012-0001
IC18	74LS74	010-0055
IC19-20	74LS136	010-0050
IC21	74LS10	010-0063
IC22-23	74LS164	010-0043
IC24	74LS139	010-0118
IC25	74LS367	010-0108
IC26	74LS139	010-0118
IC27	74LS393	010-0141
IC28-29	75452	010-0147
Optical Isolators		
OPTO1-26	MCT-66	012-0010
Transistors/Diodes		
D1-8	1N4001	008-0009
Q1	2N3904	003-0001
Q2		NOT USED
Relays		
RY1-8	SIGMA 5VDC	013-0019
IC Sockets		
4 EA.	8 PIN	017-0000
10 EA.	14 PIN	017-0001
16 EA.	16 PIN	017-0002
8 EA.	20 PIN	017-0004
Documentation		
4PIO INSTRUCTION MANUAL		023-0079

Part Description		Part No.
Resistors		
R1	180	001-0009
R2	10K	001-0030
R3	1K	001-0018
R4		NOT USED
R5	4.7K	001-0024
R6	270	001-0011
R7	10K	001-0030
R8	270	001-0011
R9	1K	001-0018
Capacitors		
C1	.1 UF @ 10V	004-0030
C2-4	.001 UF DISC	004-0022
C5-22	.1 UF @ 10V	004-0030
C23-25	10 UF @ 20V	004-0032
C26	220 PF DISC	004-0013
C27	10 UF @ 20V	004-0032
C28-35	.1 UF @ 10V	004-0030
Resistor Networks		
RN1	10K, 10 PIN	003-0024
RN2	180, 8 PIN	003-0002
RN3-4	180, 10 PIN	003-0028
RN5	10K, 10 PIN	003-0024
RN6-7	180, 10 PIN	003-0028
RN8	10K, 10 PIN	003-0024
RN9	180, 10 PIN	003-0028
RN10	180, 10 PIN	003-0028
RN11	10K, 10 PIN	003-0024
RN12-13	180, 8 PIN	003-0002
RN14	10K, 10 PIN	003-0024
RN15	1K, 10 PIN	003-0011
Miscellaneous		
8 POS. DIP SWITCH		013-0002
4 EA. 6-32X3/8 SCREW		015-0006
4 EA. 6-32 HEX NUT		015-0013
WAKEFIELD HEATSINK		021-0017
4PIO PC BOARD		020-0036
4 EA. CABLE CONNECT.		017-0012

Monsanto

DUAL PHOTOTRANSISTOR OPTO-ISOLATOR

MCT66

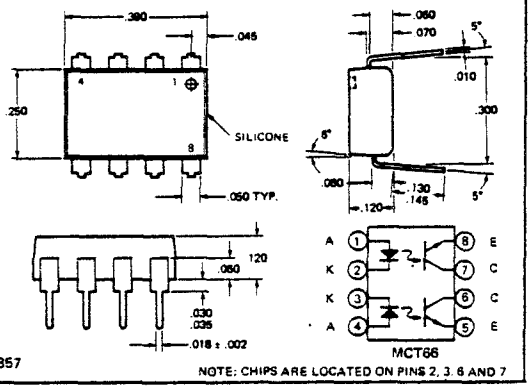
PRODUCT DESCRIPTION

The MCT66 opto-isolator has two channels for high density applications. For four channel applications, two-packages fit into a standard 16-pin DIP socket.

At the input, a GaAsLITE emitting diode generates infrared light proportional to current passing through the diode in the forward direction. At the output, a silicon phototransistor detects and amplifies the photocurrent generated in its photosensitive base region. Light coupling electrically isolates the input from the output.

PACKAGE DIMENSIONS

ALL DIMENSIONS IN INCHES



C857

NOTE: CHIPS ARE LOCATED ON PINS 2, 3, 6 AND 7

FEATURES

- Two isolated channels per package
- Two packages fit into a 16 lead DIP socket
- Same basic electrical characteristics as MCT26
- 1500 volt isolation from non-repetitive surges
- 15% typical current transfer ratio

APPLICATIONS

- AC Line/Digital Logic . . . . . Isolate high voltage transients
- Digital Logic/Digital Logic . . . . . Eliminate spurious ground loops
- Digital Logic/AC Triac Control . . . . Isolate high voltage transients
- Twisted pair line receiver . . . . . Eliminate ground loop pick-up
- Telephone/Telegraph line receiver. . . Isolate high voltage transients
- High Frequency Power Supply Feedback Control . . . . . Maintain floating ground
- Relay contact monitor . . . . . Isolate floating grounds and transients
- Power Supply Monitor . . . . . Isolate transients and ground systems

ABSOLUTE MAXIMUM RATINGS

Storage Temperature -55°C to 150°C
Operating Temperature -55°C to 100°C
Lead Temperature (soldering, 10 sec.) 250°C

INPUT DIODE (each channel)

Rated forward current, DC	60 mA
Peak reverse current	10 μA
Reverse voltage	3.0 V
Peak forward current (1 μs pulse, 300 pps)	3 A
Power dissipation at 25°C ambient	100 mW
Derate linearly from 50°C	2 mW/°C

OUTPUT TRANSISTOR (each channel)

Power dissipation @ 25°C ambient	150 mW
Derate linearly from 25°C	2 mW/°C
Collector Current	30 mA

COUPLED

Input to output breakdown voltage	1500 volts DC
Total package power dissipation @ 25°C ambient	400 mW
Derate linearly from 25°C	5.33 mW/°C

ELECTRO-OPTICAL CHARACTERISTICS (25°C Free Air Temperature Unless Otherwise Specified)

CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
INPUT DIODE					
Rated forward voltage V_F	—	1.25	1.50	V	I_F = 20 mA
Reverse voltage V_R	3.0	25	—	V	I_R = 10 μA
Reverse current I_R	—	.001	10	μA	V_R = 3.0 V
Junction capacitance C_J	—	50	—	pF	V_F = 0 V
OUTPUT TRANSISTOR (I_F = 0)					
Breakdown voltage, collector to emitter BV_{CEO}	30	85	—	V	I_C = 1.0 mA
Breakdown voltage, emitter to collector BV_{ECO}	6	13	—	V	I_C = 100 μA
Leakage current, collector to emitter I_{CEO}	—	5	100	nA	V_{CE} = 10 V
Capacitance collector to emitter C_{CE}		8		pF	V_{CE} = 0 V
COUPLED					
DC current transfer ratio (I_C/I_F) = CTR	6	15	—	%	V_{CE} = 10 V, I_F = 10 mA
Isolation voltage $BV_{(I-O)}$	1500	2500	—	VDC	Peak from non-repetitive surges
Isolation resistance $R_{(I-O)}$	10^{11}	10^{12}	—	Ω	V_{I-O} = 500 VDC
Isolation capacitance $C_{(I-O)}$	—	0.5	—	pF	f = 1 MHz
Breakdown voltage — channel-to-channel	—	1500	—	VDC	Relative humidity = 40%
Capacitance between channels	—	0.4	—	pF	f = 1 MHz
Saturation voltage — collector to emitter V_{CE} (SAT)	—	0.2	0.4	V	I_C = 2 mA, I_F = 40 mA
Bandwidth B_W	—	150	—	kHz	I_C = 2 mA, V_{CC} = 10 V, R_L = 100 Ω

ELECTRO-OPTICAL CHARACTERISTICS (Con't)

CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
SWITCHING TIMES, OUTPUT TRANSISTOR					
Non-saturated rise time, fall time (Note 3)		2.4		μs	I_C = 2 mA, V_{CE} = 10 V, R_L = 100 Ω
Non-saturated rise time, fall time (Note 3)		15		μs	I_C = 2 mA, V_{CE} = 10 V, R_L = 1 kΩ
Saturated turn-on time (from 5.0 V to 0.8 V)		5		μs	R_L = 2 KΩ, I_F = 40 mA
Saturated turn-off time (from saturation to 2.0 V)		25		μs	R_L = 2 KΩ, I_F = 40 mA

TYPICAL ELECTRO-OPTICAL CHARACTERISTIC CURVES (25°C Free Air Temperature Unless Otherwise Specified)

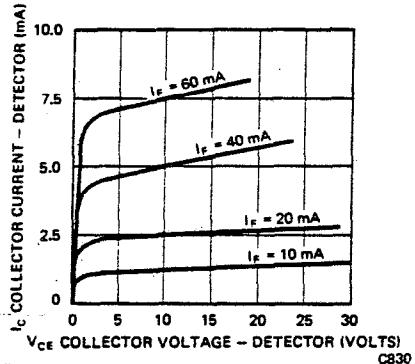


Fig. 1. Detector Output Characteristics

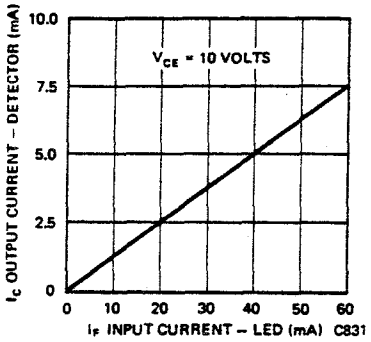


Fig. 2. Input Current vs. Output Current

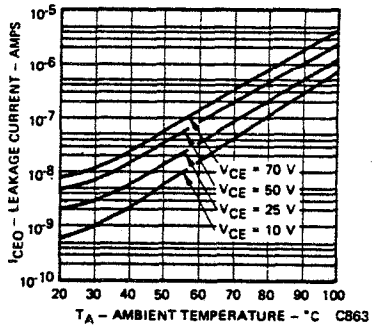


Fig. 3. Leakage Current vs. Temperature vs. Collector Voltage

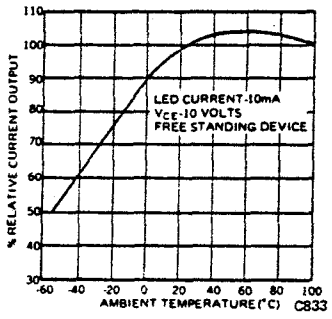


Fig. 4. Current Output vs. Temperature

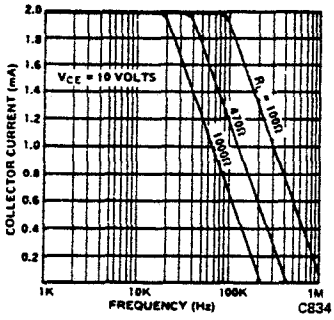


Fig. 5. Output vs. Frequency

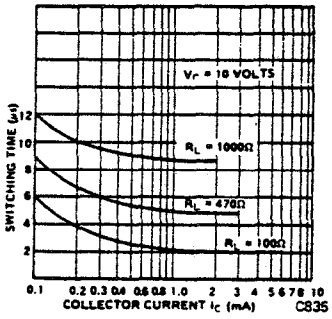


Fig. 6. Switching Time vs. Collector Current

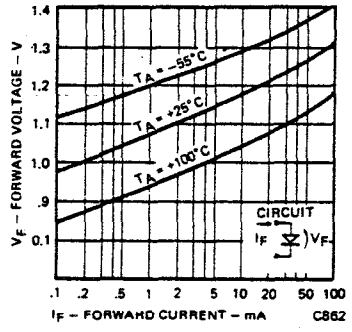


Fig. 7. I-V Curve of LED vs. Temperature

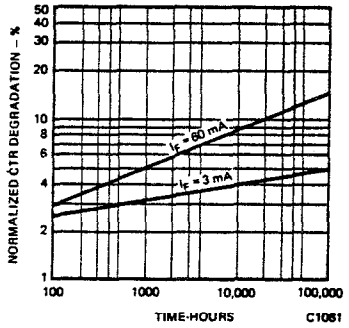
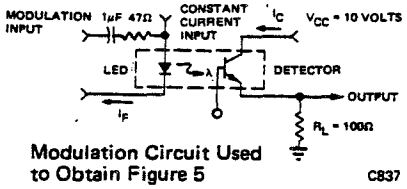
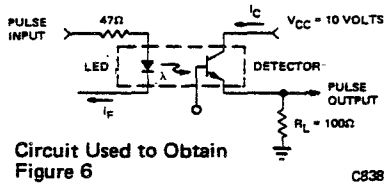


Fig. 8. Lifetime vs. Forward Current



Modulation Circuit Used to Obtain Figure 5 C837



Circuit Used to Obtain Figure 6 C838

NOTES

1. *The current transfer ratio (I_C/I_F) is the ratio of the detector collector current to the LED input current with V_{CE} at 10 volts.*
2. *The frequency at which i_c is 3 dB down from the 1 kHz value.*
3. *Rise time (t_r) is the time required for the collector current to increase from 10% of its final value to 90%.*
   Fall time (t_f) is the time required for the collector current to decrease from 90% of its initial value to 10%.

LEGEND
4PIO-020-0036
E
C
Cromemco

D1 1N4001
D2 1N4001
D3 1N4001
D4 1N4001
D5 1N4001
D6 1N4001
D7 1N4001
D8 1N4001
C28
C29
C30
C31
C32
C33
C34
C35
RY1
RY2
RY3
RY4
RY5
RY6
RY7
RY8
IC1 75452
IC2 75452
IC15 74LS273
IC28 75452
IC29 75452
R2
1K
270
R3
C22
C21
R5
1K
C27
10uF
Q4
Q1
J4
OPTO 25
OPTO 26
RN12 180
IC14 74175
C13
C20
IC27 74LS393
OPTO 23
OPTO 24
RN11 10K
IC13 74LS05
RN14 10K
IC26 74LS139
OPTO 21
OPTO 22
RN10 180
C12
IC12 74LS00
C19
IC25 74LS367
J3
OPTO 19
OPTO 20
RN9 180
C11
IC11 74LS374
C18
IC24 74LS139
OPTO 17
OPTO 18
C10
IC10 74LS244
C17
IC23 74LS164
J2
OPTO 15
OPTO 16
RN8 10K
C9
IC9 74LS374
C16
IC22 74LS164
OPTO 13
OPTO 14
RN7 180
C8
IC8 74LS374
C15
IC21 74LS10
R4
270
Q2
2N3646
OPTO 11
OPTO 12
RN6 180
C7
IC7 74LS374
IC20 74LS136
C14
C26
220
J1
OPTO 9
OPTO 10
C6
IC6 74LS374
NMI
RESET
IC19 74LS136
RN15 1K
C24
C25
OPTO 7
OPTO 8
RN5 10K
C5
IC5 74LS244
IC18 74LS74
10uF
10uF
OPTO 5
OPTO 6
RN4 180
IC4 74LS74
RN13 180
C4
IC16 7805/340T-5
OPTO 3
OPTO 4
RN3 180
R1
180
IC17 7805/340T-5
SW1
AAAAAA
765432
IC3 74LS14
OPTO 1
OPTO 2
RN2 180
RN1 10K
C2
C3
C23
10uF
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